Remarks

Claims 1-5, 8 and 21-23 are pending. Claims 6-7 and 9-20 are cancelled and new Claims 21-23 are added in this Response.

Objections to the Drawings

The Specification has been amended to include the missing part numbers noted by the Examiner in paragraph 2 of the Office Action.

Rejections Based On Ambalavanar

Claims 1-5 and 8 stand rejected as being anticipated by Ambalavanar (5,579,452) or obvious Ambalavanar in view of Kawai (5,355,441).

Claim 1 has been amended (1) to clarify that the first bus is a virtual memory address bus and the second bus is a physical memory address bus, (2) to recite that the bus masters include a print engine interface and other printer components coupled to the virtual memory address bus, and (3) to recite a printer memory coupled to the physical memory address bus. Support for the amendments to Claim 1 is found in Fig. 1 and the accompanying text at pages 4 and 5 of the Specification.

Ambalavanar teaches a virtual memory address bus (the host SBus), a physical memory address bus (the VCM VBus) and a translator (gateway 88). In Ambalavanar, the print engine interface (EPC memory 24) and the printer memory (Hard drive 34 and EPC memory 24) are all coupled to the same bus -- the physical memory address bus (the VCM VBus). Ambalavanar, Fig. 2 and column 6, lines 26-38 and lines 54-55. In Claim 1, by contrast, the print engine interface and the printer memory are coupled to different buses -- the print engine interface is coupled to the virtual memory address bus and the printer memory is coupled to the physical memory address bus. Ambalavanar and Kawai taken alone or in combination neither teach nor suggest the combination of elements recited in Claim 1.

For these reasons Claim 1 and Claims 2-5 and 8 depending from Claim 1 distinguish patentably over Ambalavanar.

New Claim 21 recites a print engine interface having a second direct memory access (DMA) controller operable to manipulate data using virtual memory addresses and a printer memory operable to store data using physical memory addresses. The print engine interface DMA controller is coupled to a virtual memory address bus while the printer

memory is coupled to a physical memory address bus. New Claim 22 recites a central processing unit, an input/output port and a print engine interface operable in a virtual memory address space and a printer memory operable in a physical memory address space. A translator is operatively coupled between the memory and the central processing unit, input/output port and print engine interface to translate virtual memory addresses from the virtual memory address space into physical memory addresses for the physical memory address space.

For the reasons detailed above for Claim 1, the cited references do not teach or suggest the combination of printer elements recited in new Claims 21 and 23.

All pending claims are now felt to be in condition for allowance. The foregoing is believed to be a complete response to the outstanding Office Action.

Respectfully submitted,
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